ABSTRACT

A computer having an instruction pipeline and profile circuitry. The profile circuitry detects and records, without compiler assistance for execution profiling, profile information describing a sequence of events occurring in the instruction pipeline. The sequence includes every event occurring during a profiled execution interval that matches time-independent selection criteria of events to be profiled. The recording continues until a predetermined stop condition is reached. The profile circuitry detects the occurrence of a predetermined condition, after a non-profiled interval of execution, and then commences the profiled execution interval.